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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,974	02/09/2004	Adnan Khaleel	NWISP049	2184

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EXAMINER	
LAU, TUNG S	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 02/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/775,974	KHALEEL, ADNAN	
	Examiner	Art Unit	
	Tung S. Lau	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32,35 and 37-46* is/are rejected.

7)☒ Claim(s) *33,34 and 36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 02/06/2006 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

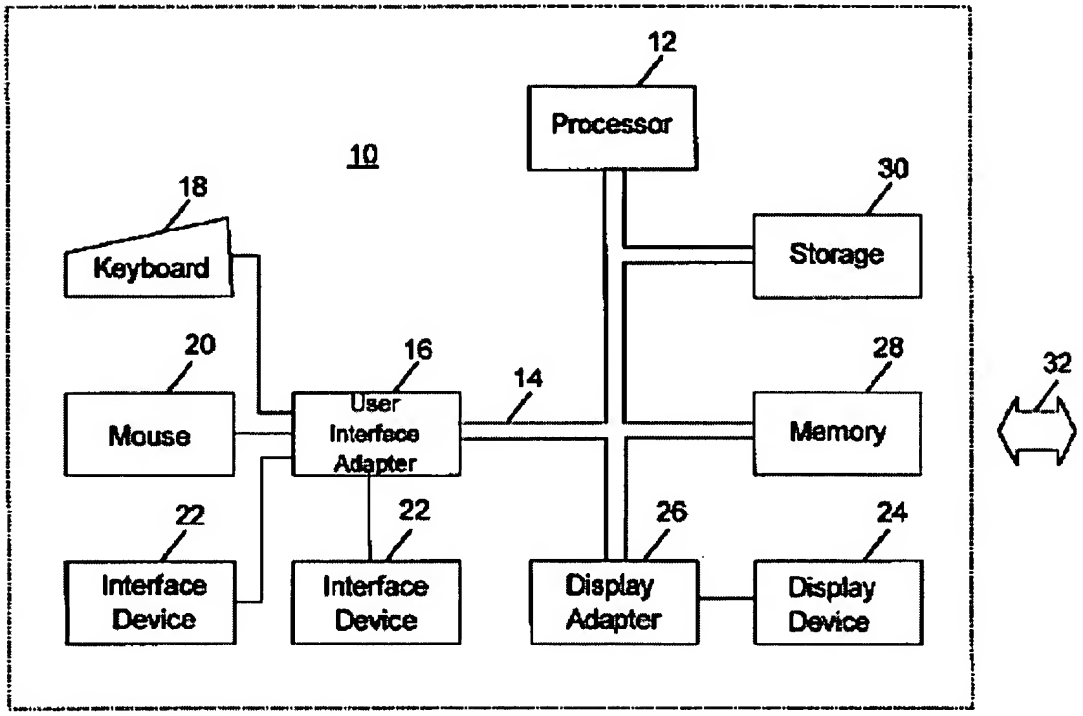
Claims 1-32, 35, and 37-46 are rejected under 35 U.S.C. 102(a) as being anticipated by Case et al. (U.S. Patent 6,601,098).

Regarding claim 1:

Case discloses a computer system comprising a processor and a memory (fig. 1, unit 28, 30, 12), the processor being operable to initiate transactions involving the memory (fig. 1, unit 28, 30, 12), the computer system further comprising a latency counter operable to generate a latency count for each of selected ones of the transactions (Col. 3-4, Lines 46-18), each latency count representing time required for completion of at least a portion of the corresponding transaction (Col.

3-4, Lines 46-18), and a plurality of histogram counters (fig. 4, unit 410, 430-450, fig. 3b, unit 300, 305), each histogram counter being operable to count selected ones of the latency counts corresponding to an associated latency range (Col. 3-4, Lines 46-18, fig. 3b, unit 300, 305).

FIG. 1

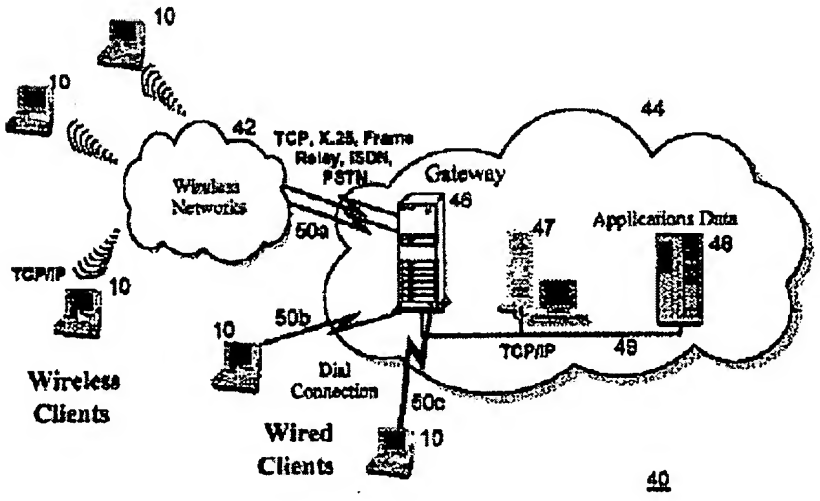


Regarding claim 22:

Case discloses an interconnection controller for use in a computer system having a plurality of processor clusters (fig. 2, unit 10, 46, 48), each cluster including a plurality of local nodes and an instance of the interconnection controller interconnected by a local point-to-point architecture (fig. 2, 42, 50b, 50c), the interconnection controller being operable to process transactions associated with the computer system (fig. 2, unit 46, 48), the interconnection controller further

comprising a latency counter (Col. 3-4, Lines 46-18) operable to generate a latency count for each of selected ones of the transactions (Col. 3-4, Lines 46-18), each latency count representing time required for completion of at least portion of the corresponding transaction and a plurality of histogram counters (Col. 3-4, Lines 46-18), each histogram counter being operable to count selected ones of the latency counts corresponding to an associated latency range (Col. 3-4, Lines 46-18, fig. 3b, unit 300, 305, fig. 4, unit 410, 430-450).

FIG. 2
(Prior Art)

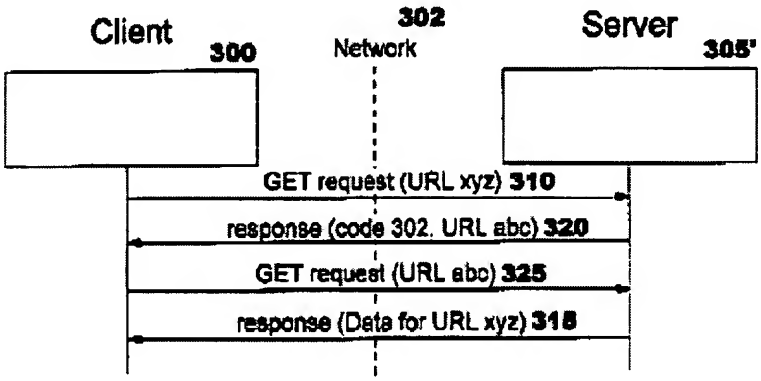


Regarding claim 38:

Case discloses a computer-implemented method for measuring performance of a computer system, comprising: generating a latency count (Col. 3-4, Lines 46-18, fig. 3b, unit 300, 305, fig. 4, unit 410, 430-450) for each of a plurality of transactions in the computer system (Col. 3-4, Lines 46-18, fig. 3b, unit 300, 305,

fig. 4, unit 410, 430-450), each latency count representing time required for completion of at least a portion of the corresponding transaction; and counting selected ones of the latency counts corresponding to each of a plurality of latency ranges, thereby generating latency distribution data (Col. 3-4, Lines 46-18, fig. 3b, unit 300, 305, fig. 4, unit 410, 430-450).

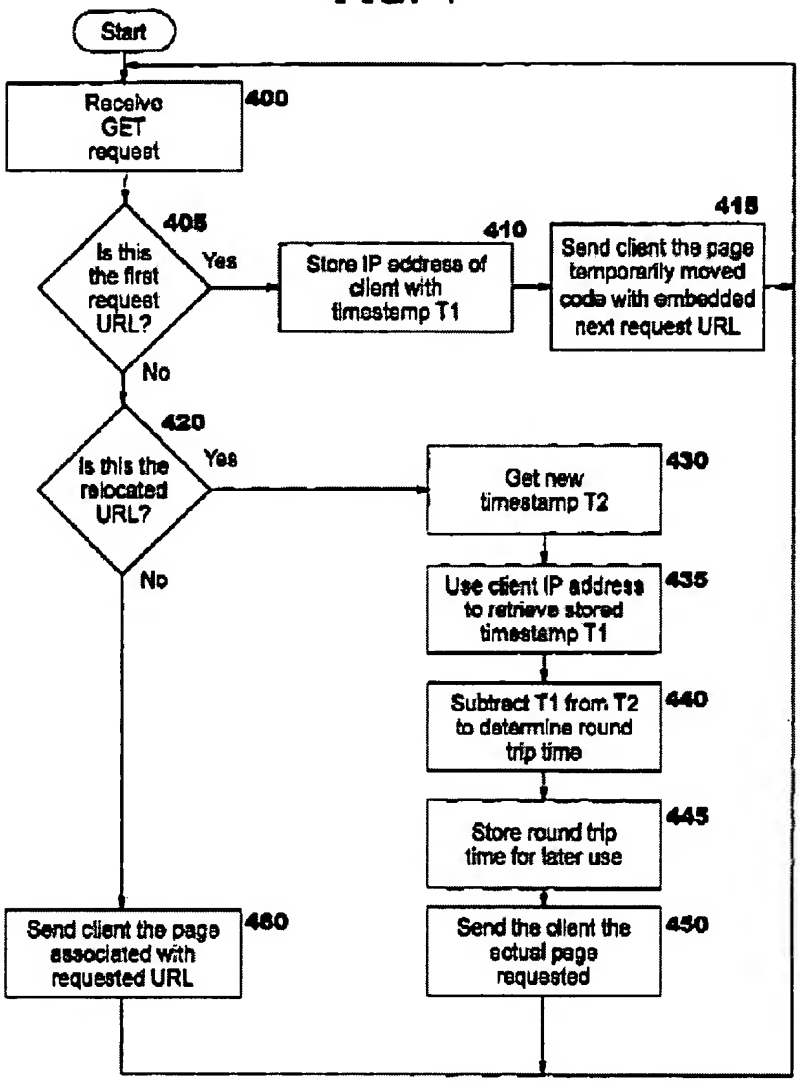
FIG. 3B



Regarding claim 41:

Case discloses an electronic system characterized by a plurality of transactions, the electronic system comprising a latency counter operable to generate a latency count (fig. 3b, unit 300, 305) for each of selected ones of the transactions (Col. 3-4, Lines 46-18, fig. 3b, unit 300, 305, fig. 4, unit 410, 430-450), and a plurality of histogram counters, each histogram counter being operable to count selected ones of the latency counts corresponding to an associated latency range (Col. 3-4, Lines 46-18, fig. 3b, unit 300, 305, fig. 4, unit 410, 430-450).

FIG. 4



Regarding claims 2, 23, Case discloses each histogram is programmable (fig. 3b, unit 310, 320, 325, 325); Regarding claims 3, 24, Case discloses each of the latency ranges is part of a window, a beginning value of the window being programmable (fig. 4, unit 430-450); Regarding claims 4, 25, Wilson discloses the latency counter is operable to count clock cycles between a first event and a second event associated with each of the selected transactions, the latency

count for each of the selected transactions corresponding to a number of clock cycles (fig. 3b, unit 310, 320, 325, 325); Regarding claim 5, Case discloses first and second events is programmable (fig. 3b, unit 310, 320, 325, 325); Regarding Claim 6, Case discloses generating transaction type (fig. 3b, unit 310, 320, 325, 325); Regarding claim 7, Case discloses the latency counter is one of plurality of latency counters, each latency counter being operable to generate the latency count for a portion of the selected transactions (fig. 3b, unit 310, 320, 325, 325); Regarding claims 8, 27, Case discloses the latency counter and the histogram counters are operable to generate and count the latency counts at run-time (fig. 3b, unit 310, 320, 325, 325); Regarding claims 9, 28, Case discloses the processor is operable to alter a run-time parameter in response to latency information derived from the histogram counters (fig. 3b, unit 310, 320, 325, 325); Regarding claim 10, Case discloses the processor is one of a plurality of processors operable to initiate the transactions (fig. 1, unit 10, 46); Regarding claim 11, Case discloses the processors and memory are interconnected with a point-to-point architecture (fig. 2, unit 10, 46, fig. 1, unit 28, 30); Regarding claim 12, Case discloses the processors and memory are interconnected with a shared-bus architecture (fig. 2, unit 10, 46, fig. 1, unit 28, 30); Regarding claim 13, Case discloses the processors are configured in a plurality of processor clusters, each cluster including a plurality of local nodes and an interconnection controller interconnected by a local point-to-point architecture, the interconnection controllers being operable to facilitate interaction among the

clusters, and wherein the latency and histogram counters are implemented in each of the interconnection controllers (fig. 2, unit 10, 46, fig. 1, unit 28, 30); Regarding claim 14, Case discloses the interconnection controller in each cluster comprises a plurality of protocol engines for processing the transactions, and wherein at least one of the interconnection controller and the local nodes in each cluster is operable to map the transactions to the protocol engines according to destination information associated with the transactions, and wherein the latency and histogram controllers are implemented in each of the protocol engines (fig. 2, unit 10, 46, fig. 1, unit 28, 30, fig. 3b, unit 300, 305).

Regarding claim 15, Case discloses the plurality of protocol engines in each interconnection controller comprises at least one remote protocol engine for processing first ones of the transactions targeting remote memory, and at least one local protocol engine for processing second ones of the transactions targeting local memory (fig. 2, unit 10, 46, fig. 1, unit 28, 30); Regarding claim 16, Case discloses the plurality of protocol engines in each interconnection controller comprises at least one remote protocol engine for processing first ones of the transactions targeting remote memory, and at least one local protocol engine for processing second ones of the transactions targeting local memory (fig. 2, unit 10, 46, fig. 1, unit 28, 30, fig. 3b, unit 300, 305); Regarding claim 17, Case discloses the interconnection controllers are further operable to facilitate cache coherency across the computer system (fig. 4, unit 430-450); Regarding claim

18, Case discloses, an input/output (I/0) device (fig. 2, unit 42), wherein the processor is further operable to generate second transactions involving the I/0 device (fig. 2, unit 42), and wherein the latency counter is further operable to generate second latency counts for selected ones of the second transactions, and wherein the plurality of histogram counters are each operable to count selected ones of the second latency counts corresponding to the associated latency range fig. 4, unit 430-450, Col. 3-4, Lines 46-18); Regarding claim 19, Case discloses based on clock cycles (fig. 4, unit 430-450); Regarding claim 20, Case discloses events are programmable (fig. 3b, unit 310-315); Regarding claim 21, Case discloses transaction type (fig. 4, unit 430-450); Regarding claim 26, Case discloses the latency counter is one of a plurality of latency counters (fig. 4, unit 430-450), each latency counter being operable to generate the latency count for a portion of the selected transactions (fig. 4, unit 430-450); Regarding claim 29, Case discloses the latency counter is one of a plurality of latency counters, each latency counter being operable to generate the latency count for a portion of the selected transactions (fig. 4, unit 430-450); Regarding claim 30, Case discloses interconnect controller (fig. 2, unit 46); Regarding claim 31, Case discloses an application specific IC (fig. 1, unit 16, 26, 28, 22, 12); Regarding claim 32, Case discloses data structure stored therein representative of interconnect controller (fig. 2, unit 110-122); Regarding claim 35, Case discloses code description (fig. 4, unit 430-450, fig. 1, unit 12); Regarding claim 39, Case discloses altering a run-time parameter (fig. 4, unit 430-450); Regarding claim 40,

Case discloses related to placement algorithm (fig. 4, unit 430-450); Regarding claims 42, 45, Case discloses counter is programmable (fig. 3b, unit 310-325); Regarding claim 43, Case discloses beginning of a value (fig. 3, unit 410); Regarding claim 44, Case discloses associated first and second events (fig. 4, unit 430-450); Regarding claim 46, Case discloses the plurality of histogram counters are operable together to generate latency distribution data, the electronic system further comprising a processor which is operable to dynamically alter a run-time parameter of the electronic system in response to the latency distribution data (fig. 4, unit 430-450, Col. 3-4, Lines 46-44), Regarding claim 37, Case discloses, at least masks portion of the interconnect controller (Col. 2-3, Lines 48-15, Col. 3-4, Lines 46-18, fig. 2, unit 46).

Allowable Subject Matter

3. Claim 33, 34 and 36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all the limitation of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance: prior art fail to teach regarding claim 33, a simulatable representation interconnect controller. Regarding claim 36, the code description corresponds to a hardware description language. .

Claim 34 is objected due to their dependency on claim 33.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

4. Applicant's arguments with respect to the amended claims have been considered but are moot in view of the new ground(s) of rejection. However, applicant's arguments filed 02/06/2006 have been fully considered but they are not persuasive.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung S Lau whose telephone number is 571-272-2274. The examiner can normally be reached on M-F 9-5:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on 571-272-2269. The fax phone numbers for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TL

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